FORM PTO-1449 (REV. 6-89)	U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office	Attorney's Docket No. 21192-06625	Application No. 10/040,852
INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		Applicant Tommy K. Eng	
		Filing Date December 28, 2001	Group Art Unit 2825

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U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If
TP	A1	5,870,308	02/09/99	Dangelo	395	500.02	
TD	A2	5,572,437	11/05/96	Rostoker et al.	364	489	
TD	A3	5,572,436	11/05/96	Dangelo et al.	364	489	
TD	A4	5,557,531	09/17/96	Rostoker et al.	364	489	
TD	A5	5,555,201	09/10/96	Dangelo et al.	364	489	
TD	A6	5,553,002	09/03/96	Dangelo et al.	364	489	
TP	A7	5,544,067	08/06/96	Rostoker et al.	364	489	
TD	A8	5,544,066	08/06/96	Rostoker et al.	364	489	
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TD	A10	5,537,580	07/16/96	Giomi et al.	395	500	
TP	A11	5,530,841	06/25/96	Gregory et al.	395	500	
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		Document Number	Date	Country	Class	Subclass	Translation Yes	No
TD	B1	WO 96/02038	01/25/96	PCT	G06F	17/50		
TD	B2	0 539 641	05/05/93	EP	G06F	15/60		

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TD	C1	Alpert, C. J. et al., "Quadratic Placement Revisited," Association for Computing Machinery, Inc., Design Automation Conference, pp. 752-757, June 1997.
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TD	C3	Kumar, T. et al., "Hierarchical Behavioral Partitioning for Multicomponent Synthesis," Proceedings Euro-Dac '96, European Design Automation Conference with Euro-VHDL '96 and Exhibition (CAT No. 96CB36000), pp. 212-217, Los Alamitos, CA., September 1996.
TD	C4	Nair, R. et al., "Generation of Performance Constraints for Layout," IEEE Transactions on Computer-Aided Design, Vol. 8, No. 8, pp. 860-874, August 1989.
TD	C5	Shahid, Kham, "RTL Foorplanning Speeds Deep-Submicron Design," Computer Design, Vol. 35, No. 2, pp. 103-106, February 1996.

EXAMINER Armando	DATE CONSIDERED 8/13/03

EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PTO-1449
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TD	C7	Venkatesh, S. V., "Hierarchical Timing-Driven Floorplanning and Place and Route Using a Timing Budgeter," IEEE Custom Integrated Circuits Conference, pp. 469-472, 1995.
TD	C8	International Search Report, PCT/US99/01965, 4 pages, August 4, 1999.

EXAMINER *Miranda*	DATE CONSIDERED 8/13/03

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